TS3A5018 10-Ω Quad SPDT Analog Switch

1 Features

- Low ON-State Resistance (10 Ω)
- Low Charge Injection
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion (THD)
- 1.8-V to 3.6-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Mode (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Sample-and-Hold Circuits
- Battery-Powered Equipment
- Audio and Video Signal Routing
- Communication Circuits

3 Description

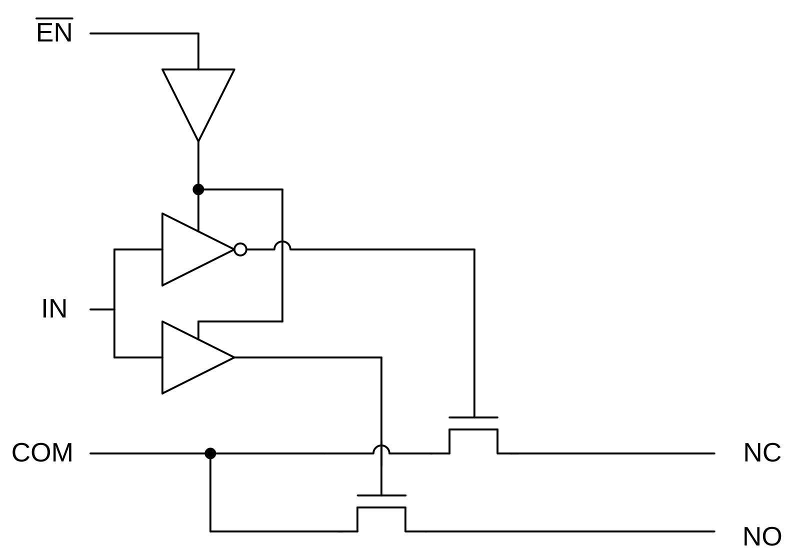
The TS3A5018 device is a quad single-pole double-throw (SPDT) analog switch that is designed to operate from 1.8 V to 3.6 V. This device can handle digital and analog signals, and signals up to V_+ can be transmitted in either direction.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS3A5018	SOIC (16)	9.90 mm × 6.00 mm
	SSOP (16)	6.00 mm × 4.90 mm
	TSSOP (16)	5.00 mm × 4.40 mm
	TVSOP (16)	4.40 mm × 3.60 mm
	UQFN (16)	2.50 mm × 1.80 mm
	VQFN (16)	4.00 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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4 Revision History

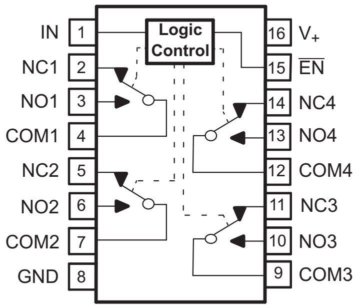
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (June 2013) to Revision G **Page**

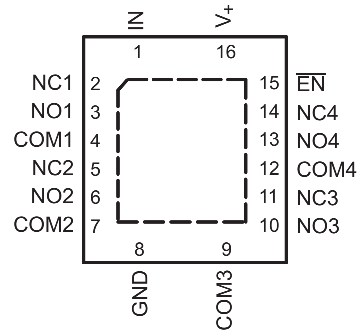
- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1
- Deleted *Ordering Information* table. 1

5 Pin Configuration and Functions

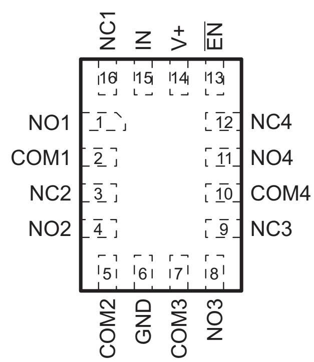
D, DBQ, DGV and PW Package
16-Pin SOIC, SSOP, TVSOP and TSSOP
(Top View)



RGY Package
16-Pin VQFN
(Top View)



RSV Package
16-Pin UQFN
(Top View)



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	SOIC, SSOP, TVSOP, VQFN NO.	UQFN NO.		
COM1	4	2	I/O	Common path for switch
COM2	7	5	I/O	Common path for switch
COM3	9	7	I/O	Common path for switch
COM4	12	10	I/O	Common path for switch
$\overline{EN}$	15	13	I	Active-low switch enable input
GND	8	6	—	Ground
IN	1	15	I	Switch path selector input
NC1	2	16	I/O	Normally closed path for switch
NC2	5	3	I/O	Normally closed path for switch
NC3	11	9	I/O	Normally closed path for switch
NC4	14	12	I/O	Normally closed path for switch
NO1	3	1	I/O	Normally open path for switch
NO2	6	4	I/O	Normally open path for switch
NO3	10	8	I/O	Normally open path for switch
NO4	13	11	I/O	Normally open path for switch
V+	16	14	—	Supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
V_+	Supply voltage(3)		–0.5	4.6	V
V_{NC} V_{NO} V_{COM}	Analog voltage(3) (4)		–0.5	4.6	V
I_K	Analog port diode current	V_{NC}, V_{NO}, V_{COM} < 0	–50		mA
I_{NC} I_{NO} I_{COM}	ON-state switch current	V_{NC}, V_{NO}, V_{COM} = 0 to 7 V	–64	64	mA
V_I	Digital input voltage(3) (4)		–0.5	4.6	V
I_{IK}	Digital input clamp current	V_I < 0	–50		mA
I_+	Continuous current through V_+		–100	100	mA
I_{GND}	Continuous current through GND		–100	100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{I/O}$	Switch input and output voltage	0	V_+	V
V_+	Supply voltage	1.65	3.6	V
V_I	Control input voltage	0	3.6	V
T_A	Operating temperature	-40	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		TS3A5018						UNIT
		D (SOIC)	DBQ (SSOP)	DGV (TVSOP)	PW (TSSOP)	RGY (VQFN)	RSV (UQFN)	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73	90	120	108	51	184	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics for 3.3-V Supply

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_+	V
r_{on}	ON-state resistance	0 ≤ (V_{NC} or V_{NO}) ≤ V_+, I_{COM} = –32 mA,	Switch ON, see Figure 17	25°C	3 V		7	10	Ω
				Full				12	
Δr_{on}	ON-state resistance match between channels	V_{NC} or V_{NO} = 2.1 V, I_{COM} = –32 mA,	Switch ON, see Figure 17	25°C	3 V		0.3	0.8	Ω
				Full				1	
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ (V_{NC} or V_{NO}) ≤ V_+, I_{COM} = –32 mA,	Switch ON, see Figure 17	25°C	3 V		5	7	Ω
				Full				8	
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current	V_{NC} or V_{NO} = 1 V, V_{COM} = 3 V, or V_{NC} or V_{NO} = 3 V, V_{COM} = 1 V,	Switch OFF, see Figure 18	25°C	3.6 V	–0.1	0.05	0.1	µA
				Full		–0.2		0.2	
		V_{NC} or V_{NO} = 0 to 3.6 V, V_{COM} = 3.6 V to 0, or V_{NC} or V_{NO} = 3.6 V to 0, V_{COM} = 0 to 3.6 V,	Switch OFF, see Figure 18	25°C	0 V	–2	0.05	2	
				Full		–10		10	
$I_{COM(OFF)}$	COM OFF leakage current	V_{COM} = 1 V, V_{NC} or V_{NO} = 3 V, or V_{COM} = 3 V, V_{NC} or V_{NO} = 3 V,	Switch OFF, see Figure 18	25°C	3.6 V	–0.1	0.05	0.1	µA
				Full		–0.2		0.2	
		V_{COM} = 0 to 3.6 V, V_{NC} or V_{NO} = 3.6 V to 0, or V_{COM} = 3.6 V to 0, V_{NC} or V_{NO} = 0 to 3.6 V,	Switch OFF, see Figure 18	25°C	0 V	–2	0.05	2	
				Full		–10		10	
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO ON leakage current	V_{NC} or V_{NO} = 1 V, V_{COM} = Open, or V_{NC} or V_{NO} = 3 V, V_{COM} = Open,	Switch ON, see Figure 19	25°C	3.6 V	–0.1	0.05	0.1	µA
				Full		–0.2		0.2	
$I_{COM(ON)}$	COM ON leakage current	V_{COM} = 1 V, V_{NC} or V_{NO} = Open, or V_{COM} = 3 V, V_{NC} or V_{NO} = Open,	Switch ON, see Figure 19	25°C	3.6 V	–0.1	0.05	0.1	µA
				Full		–0.2		0.2	
V_{IH}	Input logic high			Full		2		V_+	V
V_{IL}	Input logic low			Full		0		0.8	V
I_{IH}, I_{IL}	Input leakage current	V_I = V_+ or 0		25°C	3.6 V	–1	0.05	1	µA
				Full		–1		1	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 0.1 nF, see Figure 26	25°C	3.3 V		2		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or V_{NO} = V_+ or GND,	Switch OFF, see Figure 20	25°C	3.3 V		4.5		pF
$C_{COM(OFF)}$	COM OFF capacitance	V_{COM} = V_+ or GND,	Switch OFF, see Figure 20	25°C	3.3 V		9		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or V_{NO} = V_+ or GND,	Switch ON, see Figure 20	25°C	3.3 V		16		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND,	Switch ON, see Figure 20	25°C	3.3 V		16		pF

(1) The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Electrical Characteristics for 3.3-V Supply (continued)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
C_I	Digital input capacitance	$V_I = V_+$ or GND,	See Figure 20	25°C	3.3 V		3		pF
BW	Bandwidth	R_L = 50 Ω,	Switch ON, see Figure 22	25°C	3.3 V		300		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 10 MHz,	Switch OFF, see Figure 23	25°C	3.3 V		–48		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 10 MHz,	Switch ON, see Figure 24	25°C	3.3 V		–48		dB
$X_{TALK(ADJ)}$	Crosstalk adjacent	R_L = 50 Ω, f = 10 MHz,	Switch ON, see Figure 25	25°C	3.3 V		–81		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, see Figure 27	25°C	3.3 V		0.21%		
I_+	Positive supply current	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	3.6 V		2.5	7	µA
				Full				10	

6.6 Electrical Characteristics for 2.5-V Supply

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
V_{COM}, V_{NC}, V_{NO}	Analog signal range					0		V_+	V
r_{on}	ON-state resistance	$0 \le (V_{NC}$ or $V_{NO}) \le V_+$, I_{COM} = –24 mA,	Switch ON, see Figure 17	25°C	2.3 V		12	20	Ω
				Full				22	
Δr_{on}	ON-state resistance match between channels	V_{NC} or V_{NO} = 1.6 V, I_{COM} = –24 mA,	Switch ON, see Figure 17	25°C	2.3 V		0.3	1	Ω
				Full				2	
$r_{on(flat)}$	ON-state resistance flatness	$0 \le (V_{NC}$ or $V_{NO}) \le V_+$, I_{COM} = –24 mA,	Switch ON, see Figure 17	25°C	2.3 V		14	18	Ω
				Full				20	
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current	V_{NC} or V_{NO} = 0.5 V, V_{COM} = 2.2 V, or V_{NC} or V_{NO} = 2.2 V, V_{COM} = 0.5 V,	Switch OFF, see Figure 18	25°C	2.7 V	–0.1	0.05	0.1	µA
				Full		–0.2		0.2	
		V_{NC} or V_{NO} = 0 to 3.6 V, V_{COM} = 3.6 V to 0, or V_{NC} or V_{NO} = 3.6 V to 0, V_{COM} = 0 to 3.6 V,	Switch OFF, see Figure 18	25°C	0 V	–2	0.05	2	
				Full		–10		10	
$I_{COM(OFF)}$	COM OFF leakage current	V_{COM} = 0.5 V, V_{NC} or V_{NO} = 2.2 V, or V_{COM} = 2.2 V, V_{NC} or V_{NO} = 0.5 V,	Switch OFF, see Figure 18	25°C	2.7 V	–0.1	0.05	0.1	µA
				Full		–0.2		0.2	
		V_{COM} = 0 to 3.6 V, V_{NC} or V_{NO} = 3.6 V to 0, or V_{COM} = 3.6 V to 0, V_{NC} or V_{NO} = 0 to 3.6 V,	Switch OFF, see Figure 18	25°C	0 V	–2	0.05	2	
				Full		–10		10	
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO ON leakage current	V_{NC} or V_{NO} = 0.5 V, V_{COM} = Open, or V_{NC} or V_{NO} = 2.2 V, V_{COM} = Open,	Switch ON, see Figure 19	25°C	2.7 V	–0.1	0.05	0.1	µA
				Full		–0.2		0.2	
$I_{COM(ON)}$	COM ON leakage current	V_{COM} = 0.5 V, V_{NC} or V_{NO} = Open, or V_{COM} = 2.2 V, V_{NC} or V_{NO} = Open,	Switch ON, see Figure 19	25°C	2.7 V	–0.1	0.05	0.1	µA
				Full		–0.2		0.2	
V_{IH}	Input logic high			Full		1.7		V_+	V
V_{IL}	Input logic low			Full		0		0.7	V

(1) The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Electrical Characteristics for 2.5-V Supply (continued)

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
I_{IH}, I_{IL}	Input leakage current	$V_I = V_+$ or 0		25°C	2.7 V	–0.1	0.05	0.1	µA
				Full		–1		1	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 0.1 nF, see Figure 26	25°C	2.5 V		1		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or $V_{NO} = V_+$ or GND,	Switch OFF, see Figure 20	25°C	2.5 V		3		pF
$C_{COM(OFF)}$	COM OFF capacitance	$V_{COM} = V_+$ or GND,	Switch OFF, see Figure 20	25°C	2.5 V		9		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or $V_{NO} = V_+$ or GND,	Switch ON, see Figure 20	25°C	2.5 V		16		pF
$C_{COM(ON)}$	COM ON capacitance	$V_{COM} = V_+$ or GND,	Switch ON, see Figure 20	25°C	2.5 V		16		pF
C_I	Digital input capacitance	$V_I = V_+$ or GND,	See Figure 20	25°C	2.5 V		3		pF
BW	Bandwidth	R_L = 50 Ω,	Switch ON, see Figure 22	25°C	2.5 V		300		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 10 MHz,	Switch OFF, see Figure 23	25°C	2.5 V		–48		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 10 MHz,	Switch ON, see Figure 24	25°C	2.5 V		–48		dB
$X_{TALK(ADJ)}$	Crosstalk adjacent	R_L = 50 Ω, f = 10 MHz,	Switch ON, see Figure 25	25°C	3.3 V		–81		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, see Figure 27	25°C	2.5 V		0.33%		
I_+	Positive supply current	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	2.7 V		2.5	7	µA
				Full				10	

6.7 Electrical Characteristics for 2.1-V Supply

V_+ = 2.00 V to 2.20 V, T_A = –40°C to 85°C (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT
V_{IH}	Input logic high		Full		1.2		4.3	V
V_{IL}	Input logic low		Full		0		0.5	V

(1) The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

6.8 Electrical Characteristics for 1.8-V Supply

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
V_{COM}, V_{NC}, V_{NO}	Analog signal range					0		V_+	V
r_{on}	ON-state resistance	$0 \le (V_{NC}$ or $V_{NO}) \le V_+$, I_{COM} = –32 mA,	Switch ON, see Figure 17	25°C	1.65 V		5.5	8	Ω
				Full				14.55	
Δr_{on}	ON-state resistance match between channels	V_{NC} or V_{NO} = 1.5 V, I_{COM} = –32 mA,	Switch ON, see Figure 17	25°C	1.65 V		0.3	1	Ω
				Full				1.2	
$r_{on(flat)}$	ON-state resistance flatness	$0 \le (V_{NC}$ or $V_{NO}) \le V_+$, I_{COM} = –32 mA,	Switch ON, see Figure 17	25°C	1.65 V		2.7	5.5	Ω
				Full				7.3	

(1) The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Electrical Characteristics for 1.8-V Supply (continued)

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current	V_{NC} or V_{NO} = 0.3 V, V_{COM} = 1.65V, or V_{NC} or V_{NO} = 1.65V, V_{COM} = 0.3 V,	Switch OFF, see Figure 18	25°C	1.95 V	–0.25	0.03	0.25	µA
				Full		–4.5		4.5	
		V_{NC} or V_{NO} = 1.95 V to 0 V, V_{COM} = 0 V to 1.95 V, or V_{NC} or V_{NO} = 0 V to 1.95 V, V_{COM} = 1.95 V to 0 V,	Switch OFF, see Figure 18	25°C	0 V	–0.4	0.01	0.4	
				Full		–6.5		6.5	
$I_{COM(OFF)}$	COM OFF leakage current	V_{COM} = 1.65 V, V_{NC} or V_{NO} = 0.3V, or V_{COM} = 0.3 V, V_{NC} or V_{NO} = 1.65V,	Switch OFF, see Figure 18	25°C	1.95 V	–0.4	0.02	0.4	µA
				Full		–0.9		0.9	
		V_{COM} = 0 V to 1.95 V, V_{NC} or V_{NO} = 1.95 V to 0 V, or V_{COM} = 1.95 V to 0, V_{NC} or V_{NO} = 0 to 1.95 V,	Switch OFF, see Figure 18	25°C	0 V	–0.4	0.02	0.4	
				Full		–4.5		4.5	
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO ON leakage current	V_{NC} or V_{NO} = 0.3 V, V_{COM} = Open, or V_{NC} or V_{NO} = 1.65 V, V_{COM} = Open,	Switch ON, see Figure 19	25°C	1.95 V	–2.	0.02	2	µA
				Full		–2	0.02	2	
$I_{COM(ON)}$	COM ON leakage current	V_{COM} = 0.3 V, V_{NC} or V_{NO} = Open, or V_{COM} = 1.65 V, V_{NC} or V_{NO} = Open,	Switch ON, see Figure 19	25°C	1.95 V	–4.5		4.5	µA
				Full					
V_{IH}	Input logic high	V_I = V_+ or GND		Full	1.95 V	1		3.6	V
V_{IL}	Input logic low			Full	1.95 V	0		0.4	V
I_{IH}, I_{IL}	Input leakage current	V_I = V_+ or 0		25°C	1.95 V	–0.1	0.01	0.1	µA
				Full		–2.1		2.1	

6.9 Switching Characteristics for 3.3-V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
t_{ON}	Turnon time	V_{COM} = 2 V, R_L = 300 Ω,	C_L = 35 pF, see Figure 21	25°C	3.3 V	2.5	3.5	8	ns
				Full	3 V to 3.6 V	2.5		9	
t_{OFF}	Turnoff time	V_{COM} =2 V, R_L = 300 Ω,	C_L = 35 pF, see Figure 21	25°C	3.3 V	0.5	2	6.5	ns
				Full	3 V to 3.6 V	0.5		7	

6.10 Switching Characteristics for 2.5-V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
t_{ON}	Turnon time	V_{COM} = 1.5 V, R_L = 300 Ω,	C_L = 35 pF, see Figure 21	25°C	2.5 V	2.5	5	9.5	ns
				Full	2.3 V to 2.7 V	2.5		10.5	
t_{OFF}	Turnoff time	V_{COM} =1.5 V, R_L = 300 Ω,	C_L = 35 pF, see Figure 21	25°C	2.5 V	0.5	3	7.5	ns
				Full	2.3 V to 2.7 V	0.5		9	

6.11 Switching Characteristics for 1.8-V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
t_{ON}	Turnon time	$V_{COM} = V_+$, $R_L = 50\ \Omega$,	$C_L = 35$ pF, see Figure 21	25°C	1.8 V		14.1	49.3	ns
				Full	1.65 V to 1.95 V		49.3	56.7	
t_{OFF}	Turnoff time	$V_{COM} = V_+$, $R_L = 50\ \Omega$,	$C_L = 35$ pF, see Figure 21	25°C	1.8 V		16.1	26.5	ns
				Full	1.65 V to 1.95 V			31.2	
t_{BBM}	Break-before-make time	$V_{NC} = V_{NO} = V_+/2$, $R_L = 50\ \Omega$,	$C_L = 35$ pF, see Figure 21	25°C	1.8 V	5.3	18.4	58	ns
				Full	1.65 V to 1.95 V			58	

6.12 Typical Characteristics

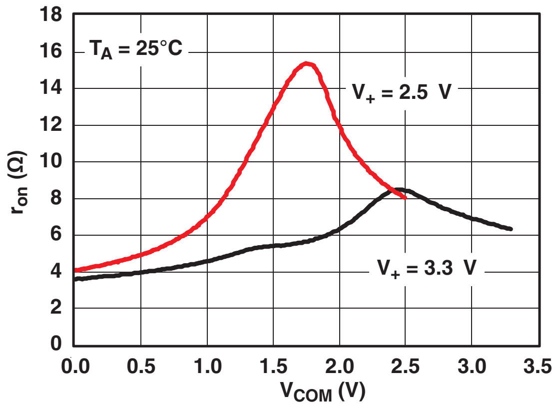


Figure 1. r_{on} vs V_{COM} (V_+ = 3.3 V)

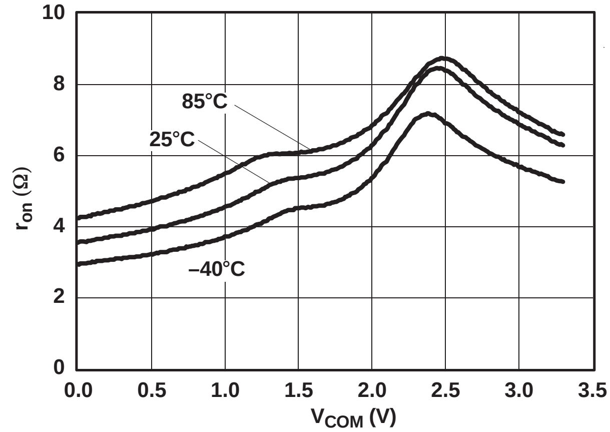


Figure 2. r_{on} vs V_{COM} (V_+ = 2.5 V)

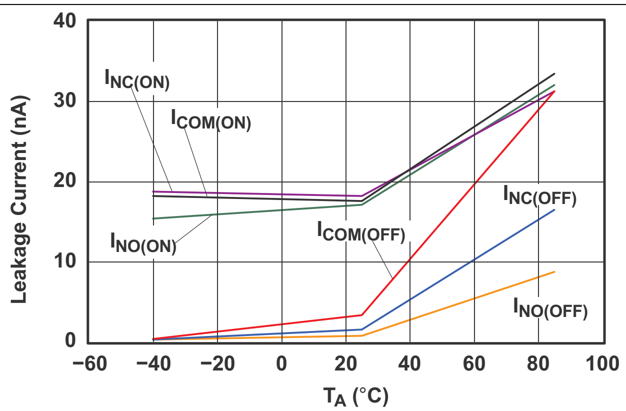


Figure 3. Leakage Current vs Temperature (V_+ = 3.6 V)

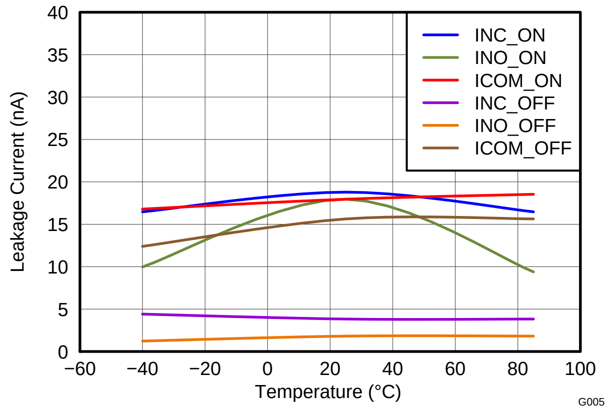


Figure 4. Leakage Current vs Temperature (V_+ = 1.8 V)

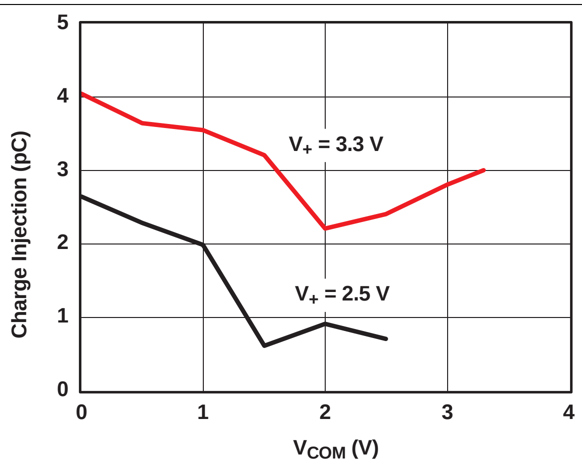


Figure 5. Charge Injection (Q_C) vs V_{COM}

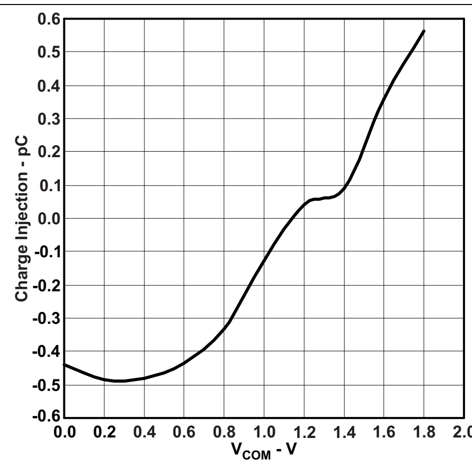


Figure 6. Charge Injection (Q_C) vs V_{COM} (V_+ = 1.8 V)

Typical Characteristics (continued)

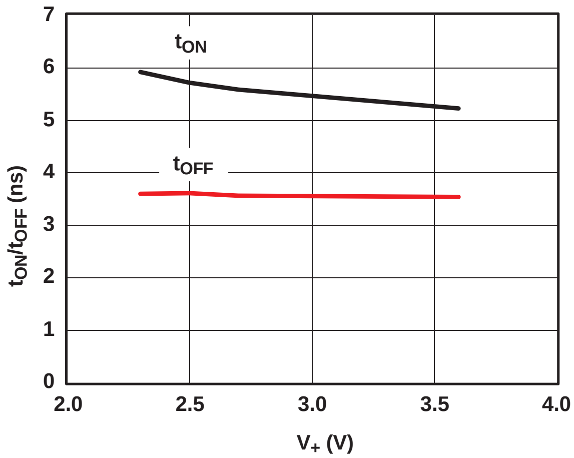


Figure 7. t_{ON} and t_{OFF} vs Supply Voltage

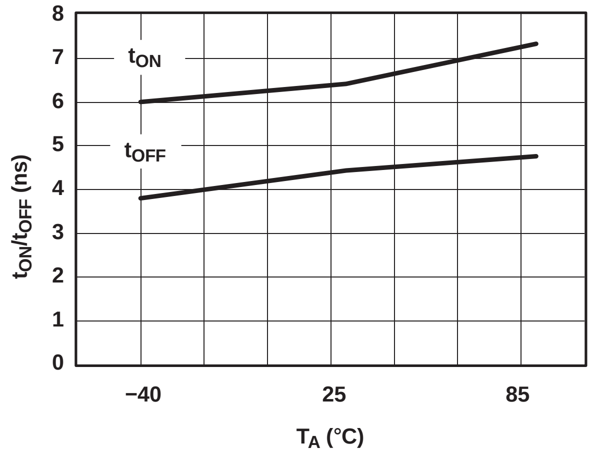


Figure 8. t_{ON} and t_{OFF} vs Temperature (V_+ = 3.3 V)

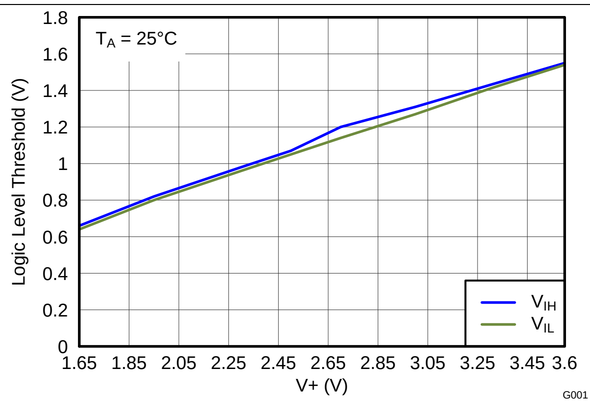


Figure 9. Logic-Level Threshold vs V_+

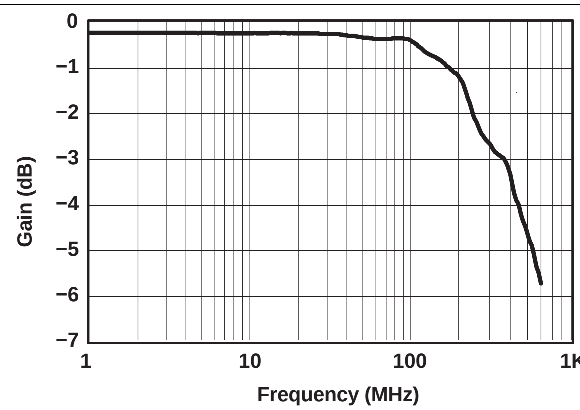


Figure 10. Gain vs Frequency Bandwidth (V_+ = 3.3 V)

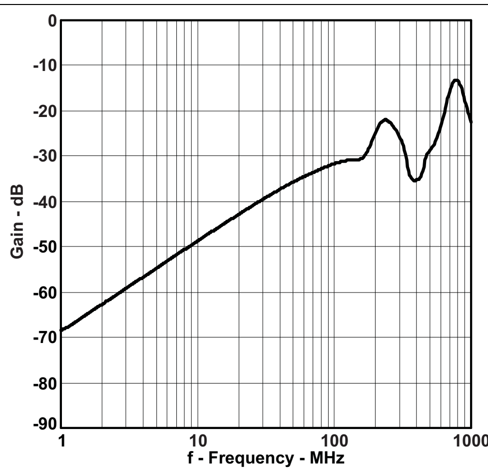


Figure 11. OFF Isolation vs Frequency (V_+ = 1.8 V)

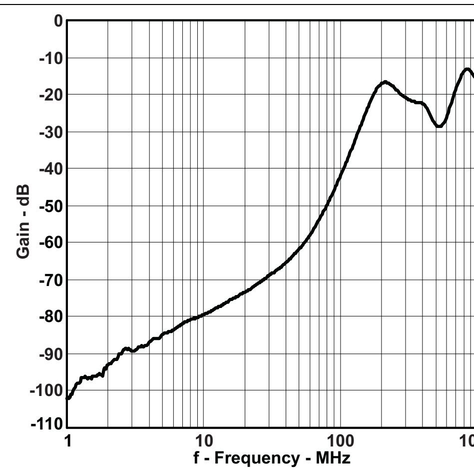


Figure 12. Crosstalk Adjacent vs Frequency (V_+ = 1.8 V)

Typical Characteristics (continued)

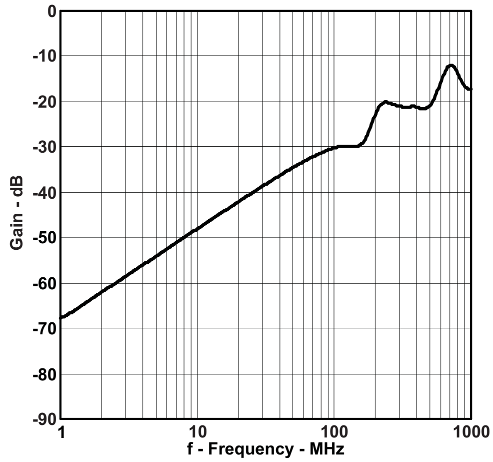


Figure 13. Crosstalk vs Frequency (V_+ = 1.8 V)

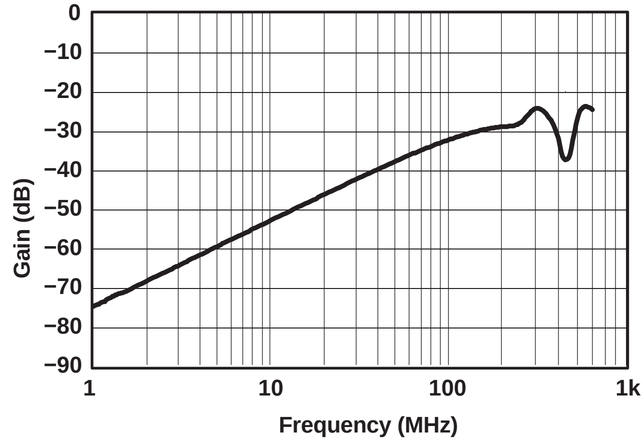


Figure 14. OFF Isolation vs Frequency (V_+ = 3.3 V)

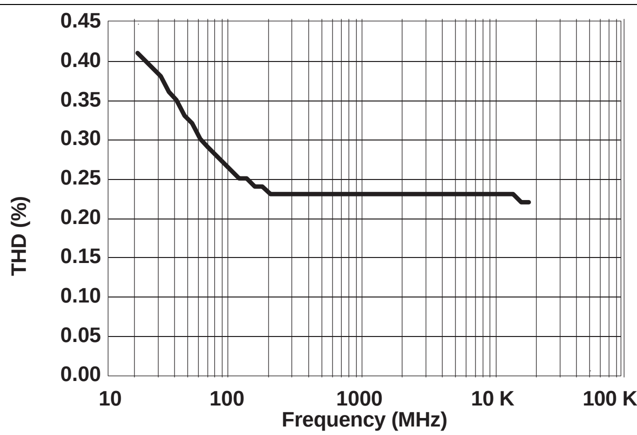


Figure 15. Total Harmonic Distortion vs Frequency

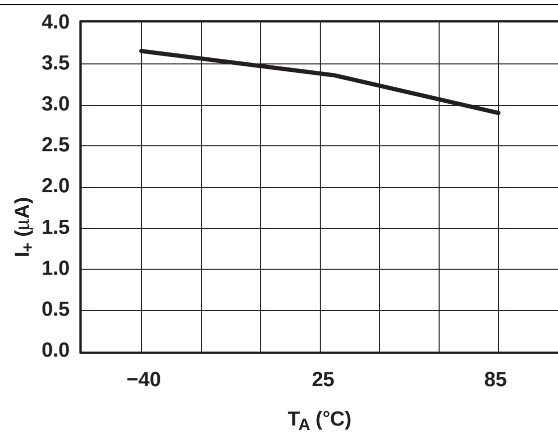


Figure 16. Power-Supply Current vs Temperature (V_+ = 3.3 V)

7 Parameter Measurement Information

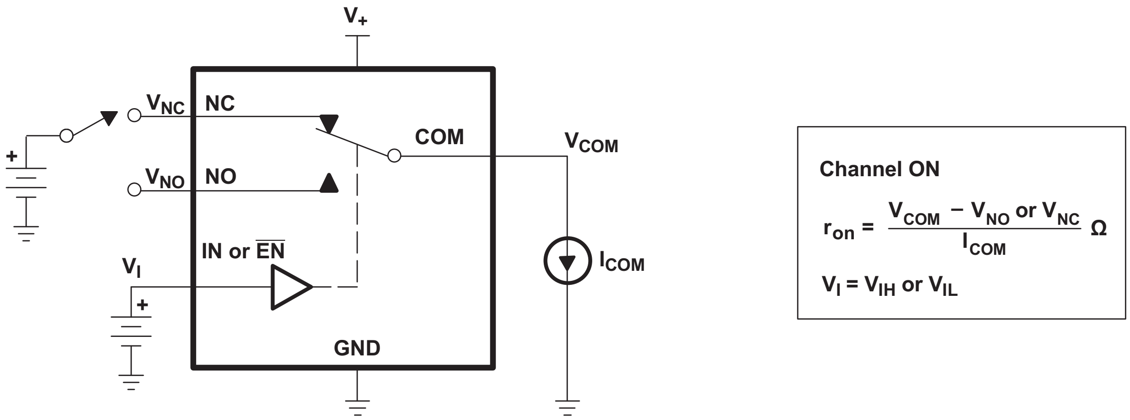


Figure 17. ON-State Resistance (r_{on})

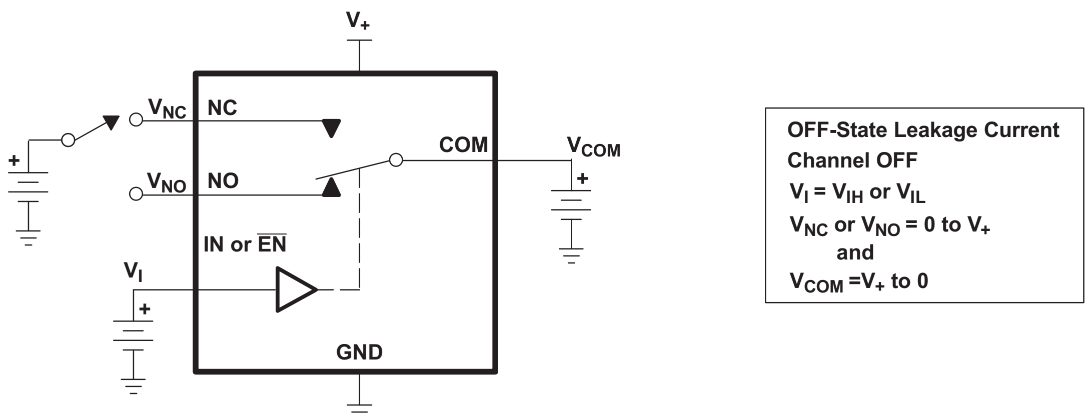


Figure 18. OFF-State Leakage Current ($I_{COM(OFF)}$, $I_{NC(OFF)}$, $I_{NO(OFF)}$)

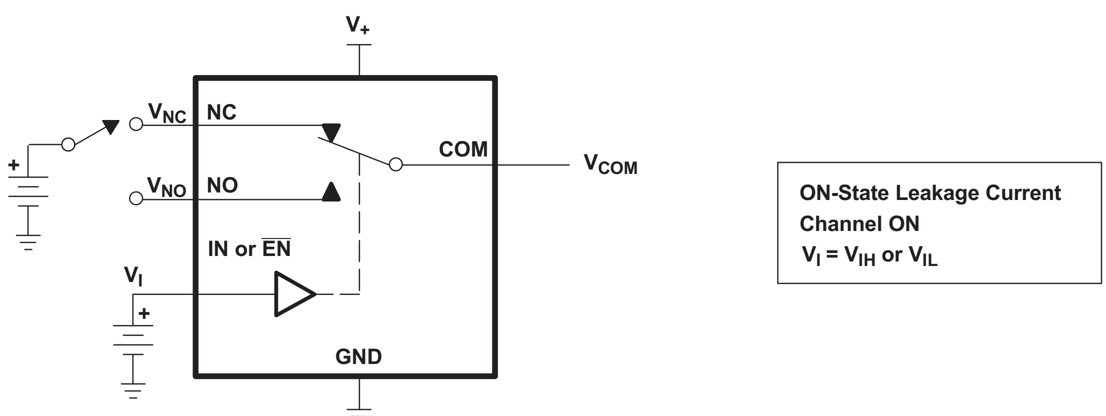


Figure 19. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$)

Parameter Measurement Information (continued)

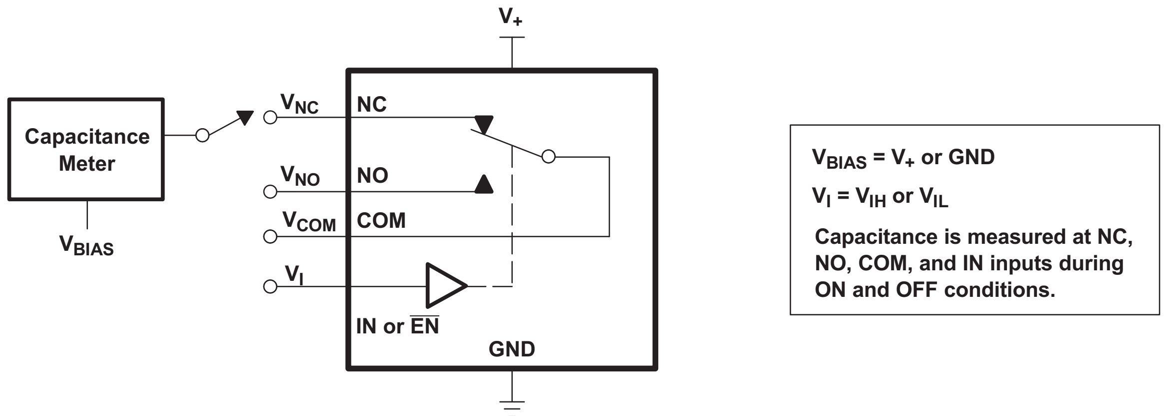
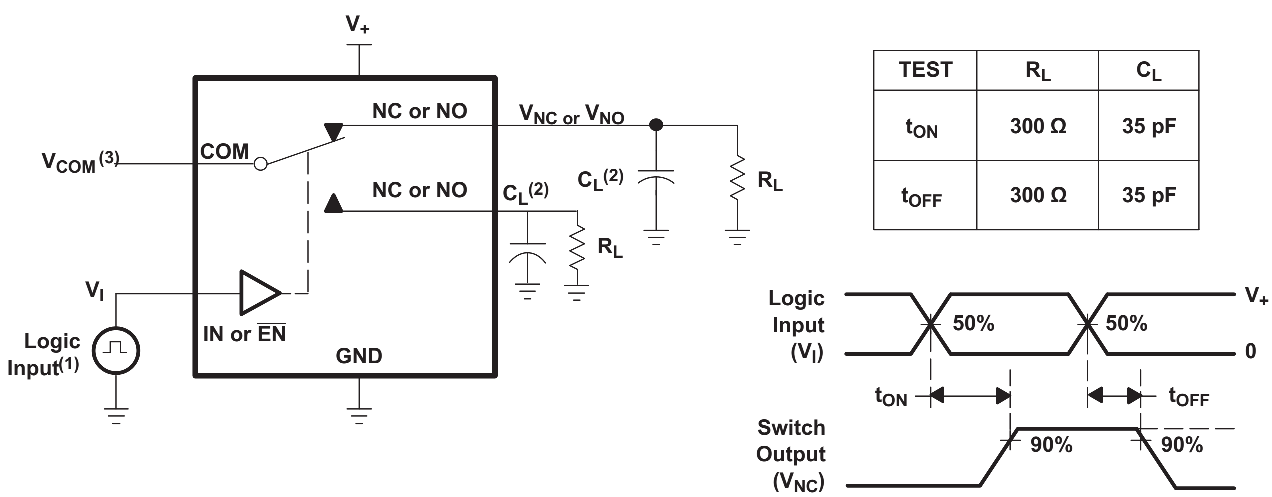


Figure 20. Capacitance (C_I, $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NC(ON)}$)



TEST	R_L	C_L
t_{ON}	300 Ω	35 pF
t_{OFF}	300 Ω	35 pF

(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

(3) See Electrical Characteristics for V_{COM}.

Figure 21. Turnon (t_{ON}) and Turnoff Time (t_{OFF})

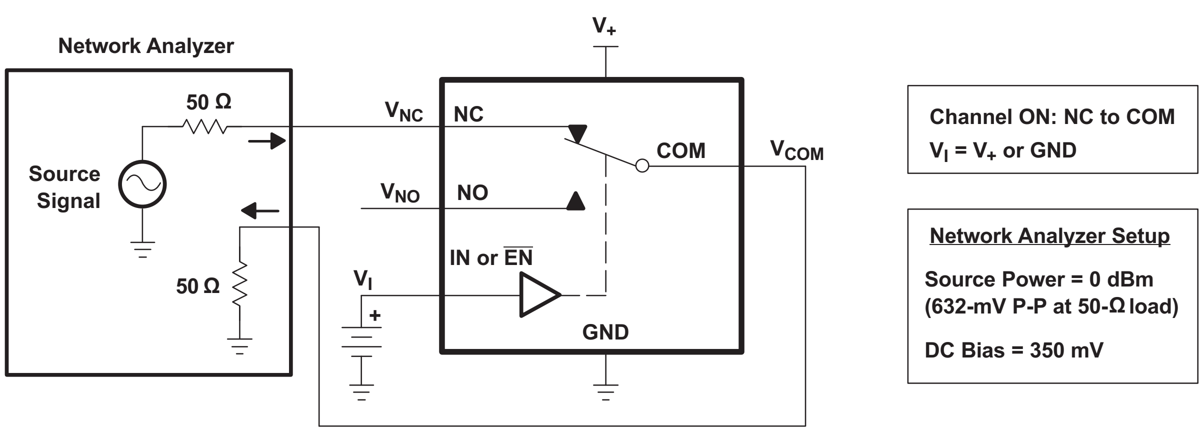


Figure 22. Bandwidth (BW)

Parameter Measurement Information (continued)

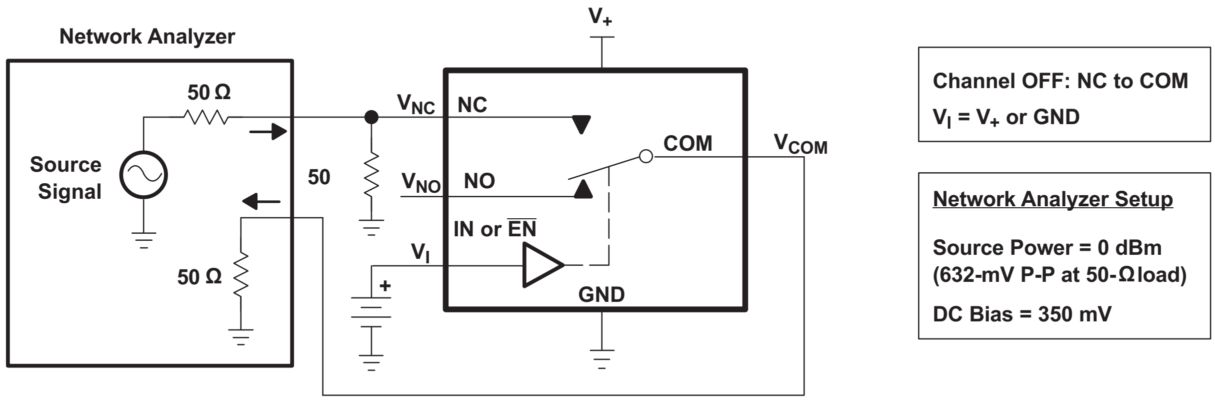


Figure 23. OFF Isolation (O_{ISO})

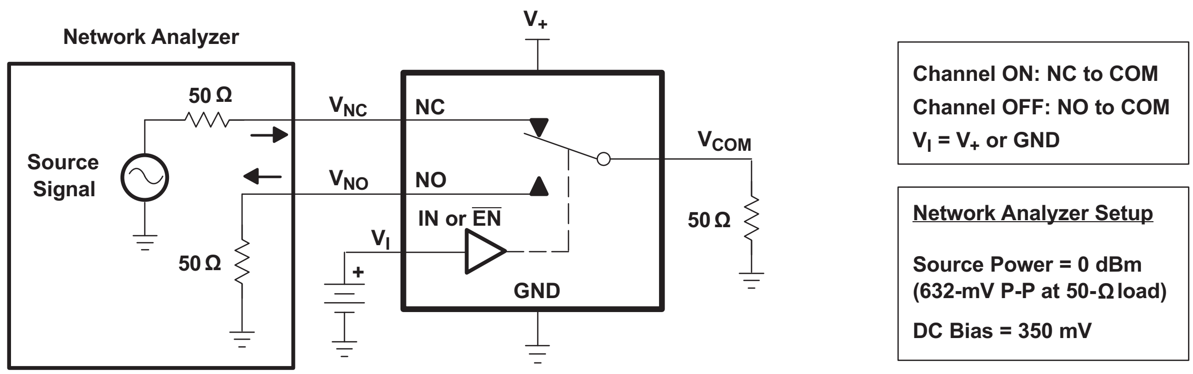


Figure 24. Crosstalk (X_{TALK})

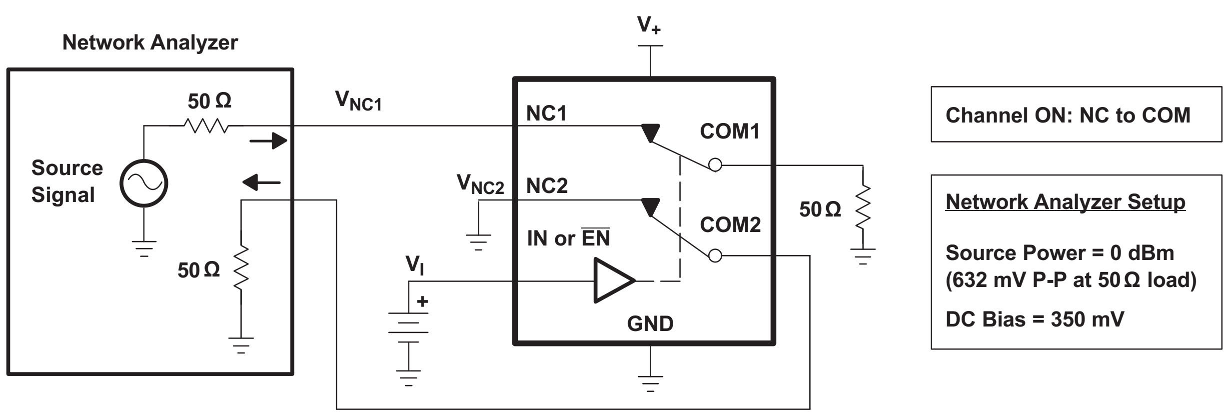
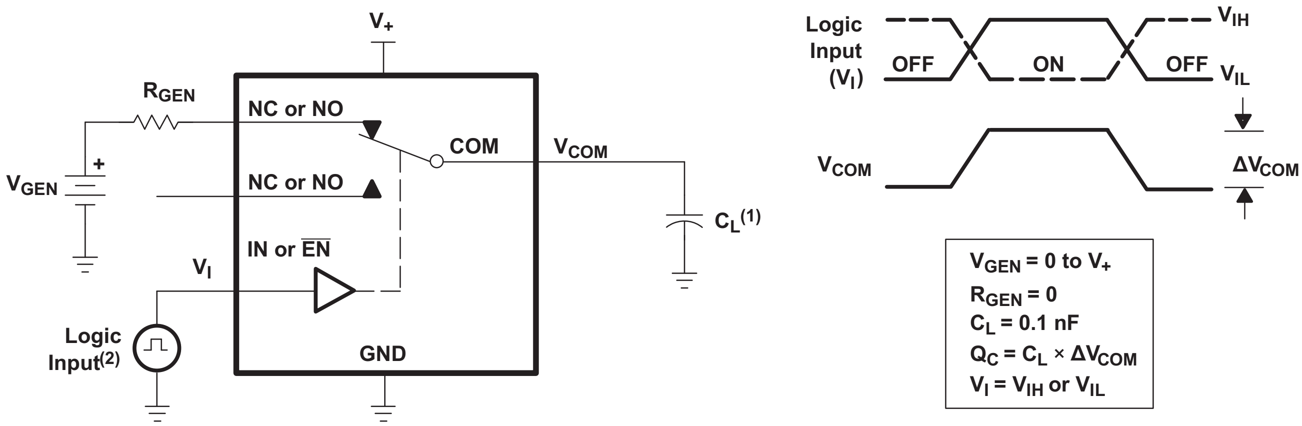


Figure 25. Crosstalk Adjacent

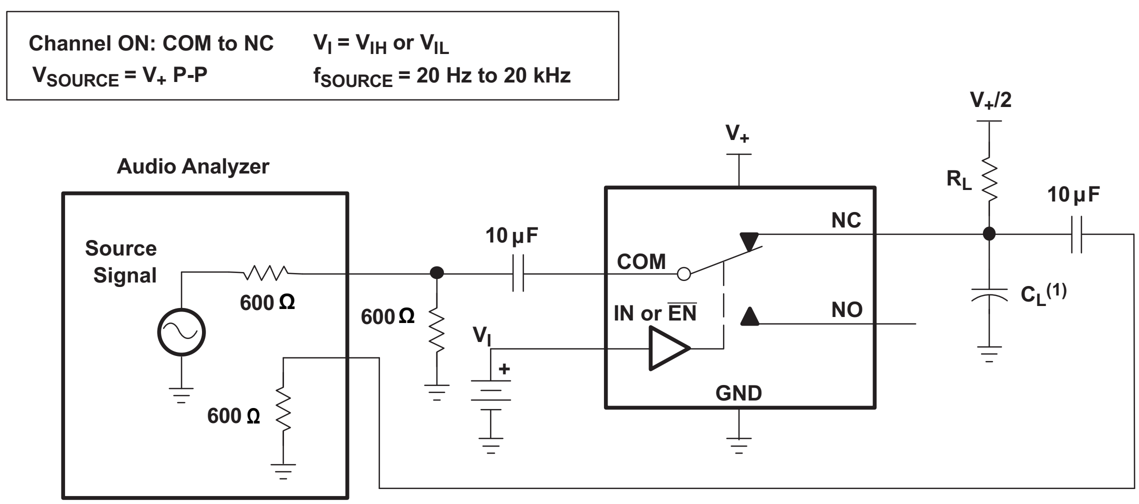
Parameter Measurement Information (continued)



(1) C_L includes probe and jig capacitance.

(2) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

Figure 26. Charge Injection (Q_C)



(1) C_L includes probe and jig capacitance.

Figure 27. Total Harmonic Distortion (THD)

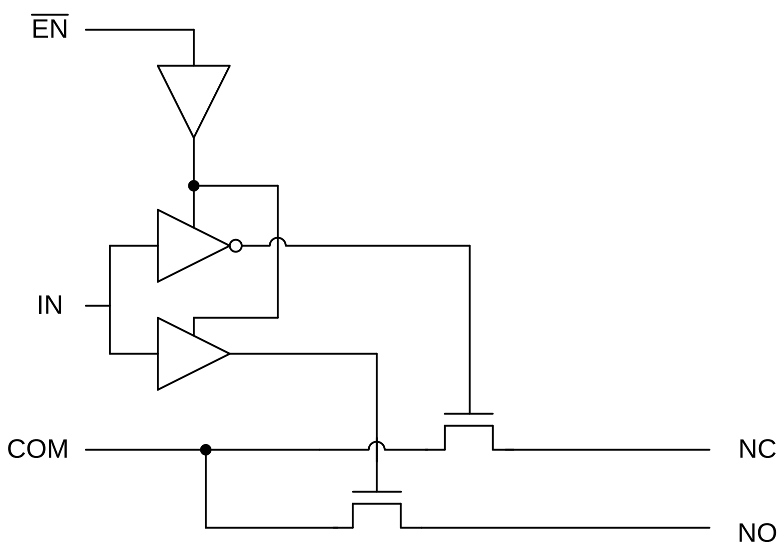
8 Detailed Description

8.1 Overview

The TS3A5018 is a quad single-pole-double-throw (SPDT) solid-state analog switch. The TS3A5018, like all analog switches, is bidirectional. When powered on, each COM pin is connected to its respective NC pin. For this device, NC stands for *normally closed* and NO stands for *normally open*. The switch is enabled when $\overline{\text{EN}}$ is low. If IN is also low, COM is connected to NC. If IN is high, COM is connected to NO.

The TS3A5018 is a break-before-make switch. This means that during switching, a connection is broken before a new connection is established. The NC and NO pins are never connected to each other.

8.2 Functional Block Diagram (Each Switch)



8.3 Feature Description

The low ON-state resistance, ON-state resistance matching, and charge injection in the TS3A5018 make this switch an excellent choice for analog signals that require minimal distortion. In addition, the low THD allows audio signals to be preserved more clearly as they pass through the device.

The 1.8-V to 3.6-V operation allows compatibility with more logic levels, and the bidirectional I/Os can pass analog signals from 0 V to V_+ with low distortion.

8.4 Device Functional Modes

Table 1. Function Table

$\overline{\text{EN}}$	IN	NO TO COM, COM TO NO	NC TO COM, COM TO NC
L	L	OFF	ON
L	H	ON	OFF
H	X	OFF	OFF

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TS3A5018 can be used in a variety of customer systems. The TS3A5018 can be used anywhere multiple analog or digital signals must be selected to pass across a single line.

9.2 Typical Application

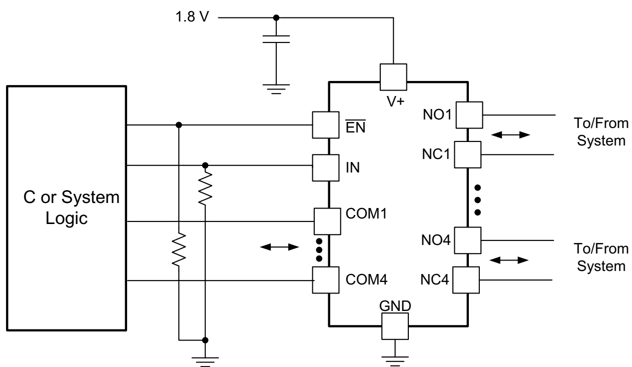


Figure 28. System Schematic for TS3A5018

9.2.1 Design Requirements

In this particular application, V_+ was 1.8 V, although V_+ is allowed to be any voltage specified in *Recommended Operating Conditions*. A decoupling capacitor is recommended on the V+ pin. See *Power Supply Recommendations* for more details.

9.2.2 Detailed Design Procedure

In this application, $\overline{EN}$ and IN are, by default, pulled low to GND. Choose these resistor sizes based on the current driving strength of the GPIO, the desired power consumption, and the switching frequency (if applicable). If the GPIO is open-drain, use pullup resistors instead.

9.2.3 Application Curve

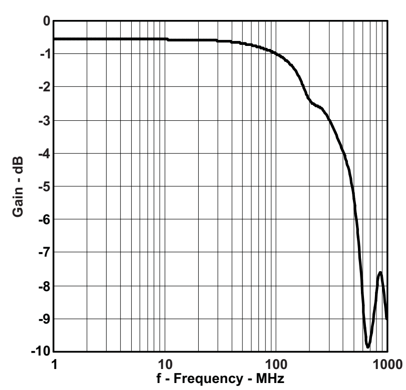


Figure 29. Gain vs Frequency Bandwidth (V_+ = 1.8 V)

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF bypass capacitor is recommended. If there are multiple pins labeled V_{CC}, then a 0.01-μF or 0.022-μF capacitor is recommended for each V_{CC} because the VCC pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-μF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self–inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. Below figure shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

Unused switch I/Os, such as NO, NC, and COM, can be left floating or tied to GND. However, the IN and $\overline{\text{EN}}$ pins must be driven high or low. Due to partial transistor turnon when control inputs are at threshold levels, floating control inputs can cause increased I_{CC} or unknown switch selection states.

11.2 Layout Example

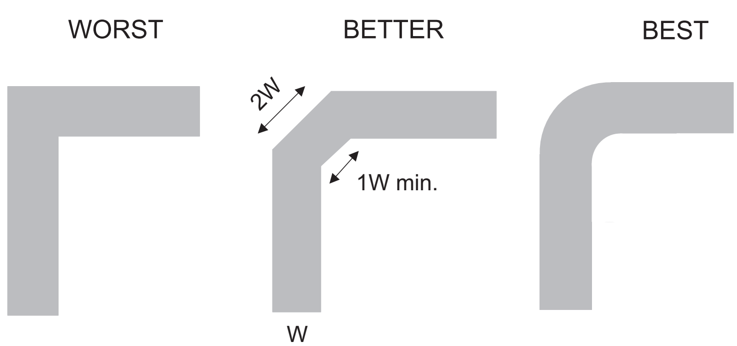


Figure 30. Trace Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

Table 2. Parameter Description

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NC}	Voltage at NC
V_{NO}	Voltage at NO
r_{on}	Resistance between COM and NC or NO ports when the channel is ON
Δr_{on}	Difference of r_{on} between channels in a specific device
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
$I_{COM(OFF)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NC or NO) in the OFF state
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NC or NO) in the ON state and the output (NC or NO) open
V_{IH}	Minimum input voltage for logic high for the control input (IN, $\overline{EN}$)
V_{IL}	Maximum input voltage for logic low for the control input (IN, $\overline{EN}$)
V_I	Voltage at the control input (IN, $\overline{EN}$)
I_{IH}, I_{IL}	Leakage current measured at the control input (IN, $\overline{EN}$)
t_{ON}	Turnon time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output NC or NO) signal when the switch is turning ON.
t_{OFF}	Turnoff time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (NC or NO) signal when the switch is turning OFF.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC or NO) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$, C_L is the load capacitance and ΔV_{COM} is the change in analog output voltage.
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
$C_{NO(OFF)}$	Capacitance at the NC port when the corresponding channel (NO to COM) is OFF
$C_{NO(ON)}$	Capacitance at the NC port when the corresponding channel (NO to COM) is ON
$C_{COM(OFF)}$	Capacitance at the COM port when the corresponding channel (COM to NC) is OFF
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NC) is ON
C_I	Capacitance of control input (IN, $\overline{EN}$)
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM) in the OFF state.
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC1 to NO1). Adjacent crosstalk is a measure of unwanted signal coupling from an ON channel to an adjacent ON channel (NC1 to NC2) .This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.
I_+	Static power-supply current with the control (IN) pin at V_+ or GND

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

- *Implications of Slow or Floating CMOS Inputs*, SCBA004

12.3 Trademarks

All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3A5018D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS3A5018	Samples
TS3A5018DBQR	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YA018	Samples
TS3A5018DBQRE4	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YA018	Samples
TS3A5018DBQRG4	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YA018	Samples
TS3A5018DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS3A5018	Samples
TS3A5018DGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YA018	Samples
TS3A5018DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS3A5018	Samples
TS3A5018DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS3A5018	Samples
TS3A5018PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YA018	Samples
TS3A5018PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YA018	Samples
TS3A5018PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YA018	Samples
TS3A5018PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YA018	Samples
TS3A5018RGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YA018	Samples
TS3A5018RGYRG4	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YA018	Samples
TS3A5018RSVR	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ZUN	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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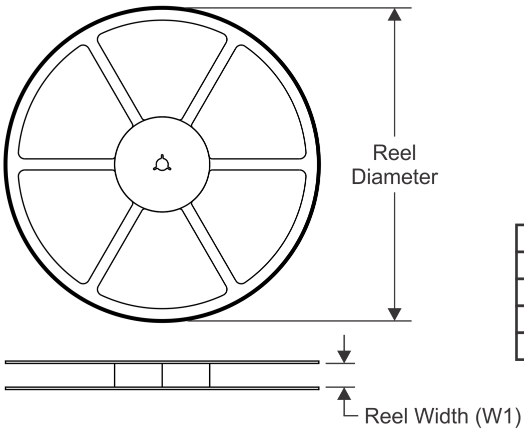
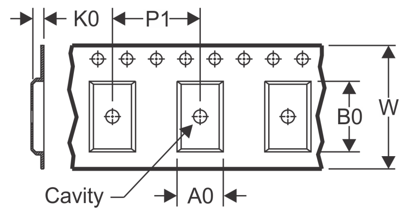
TAPE AND REEL INFORMATION

REEL DIMENSIONS

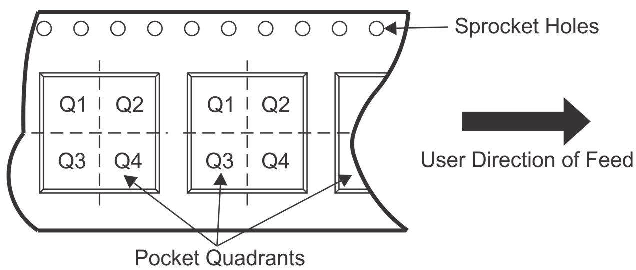


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

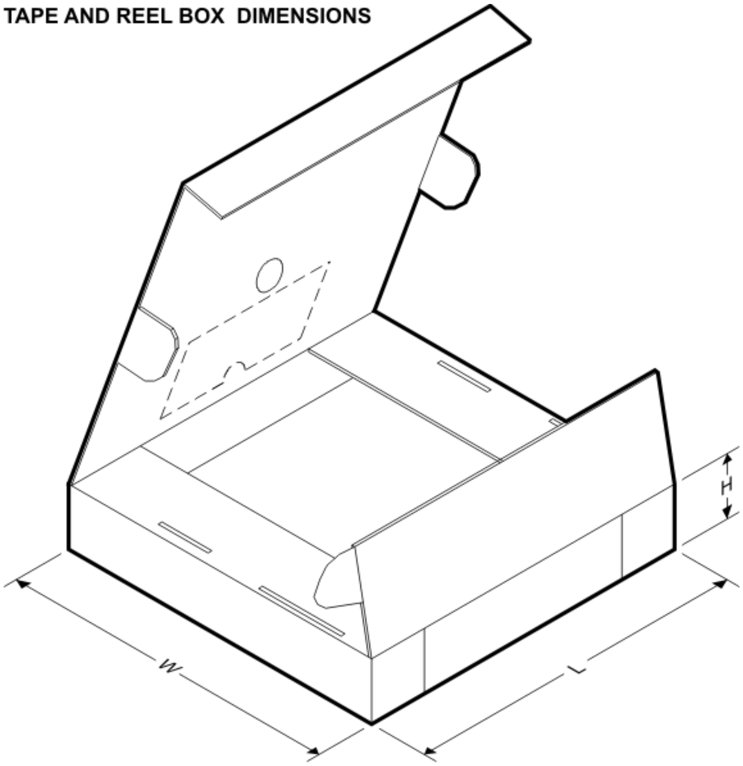
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A5018DBQR	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TS3A5018DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
TS3A5018DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TS3A5018PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TS3A5018RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
TS3A5018RSVR	UQFN	RSV	16	3000	180.0	12.4	2.1	2.9	0.75	4.0	12.0	Q1
TS3A5018RSVR	UQFN	RSV	16	3000	177.8	12.4	2.0	2.8	0.7	4.0	12.0	Q1
TS3A5018RSVR	UQFN	RSV	16	3000	180.0	13.2	2.1	2.9	0.75	4.0	12.0	Q1

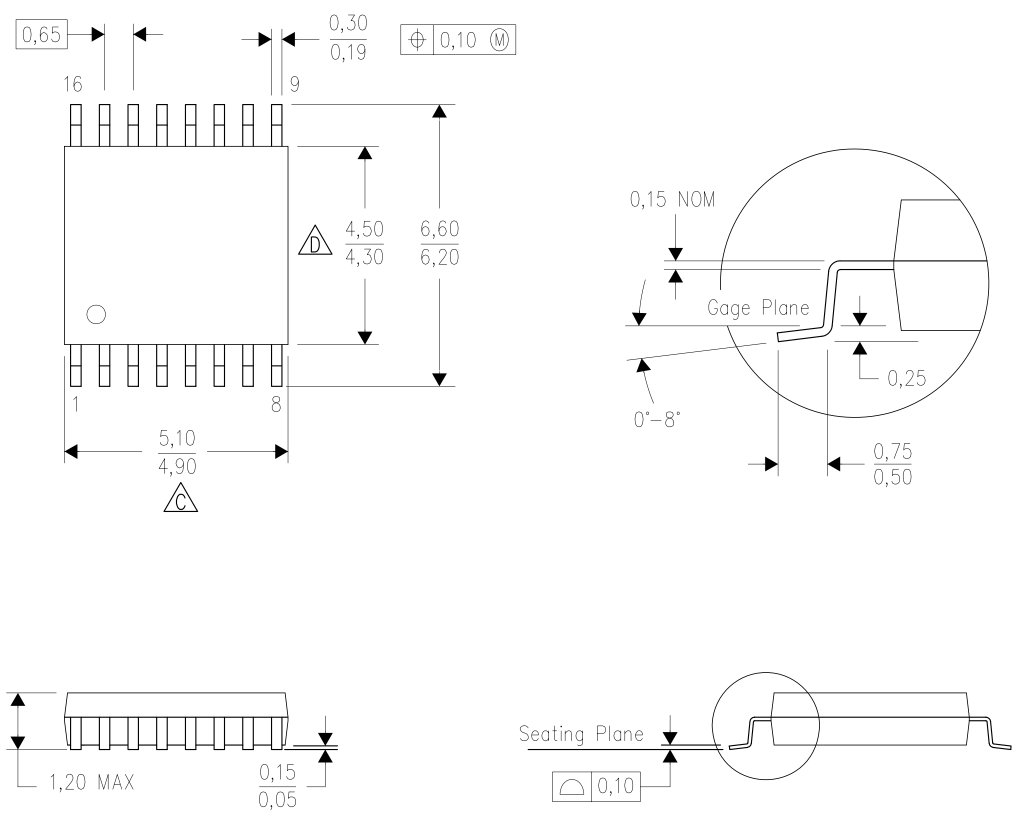
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A5018DBQR	SSOP	DBQ	16	2500	340.5	338.1	20.6
TS3A5018DGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
TS3A5018DR	SOIC	D	16	2500	333.2	345.9	28.6
TS3A5018PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
TS3A5018RGYR	VQFN	RGY	16	3000	367.0	367.0	35.0
TS3A5018RSVR	UQFN	RSV	16	3000	203.0	203.0	35.0
TS3A5018RSVR	UQFN	RSV	16	3000	202.0	201.0	28.0
TS3A5018RSVR	UQFN	RSV	16	3000	184.0	184.0	19.0

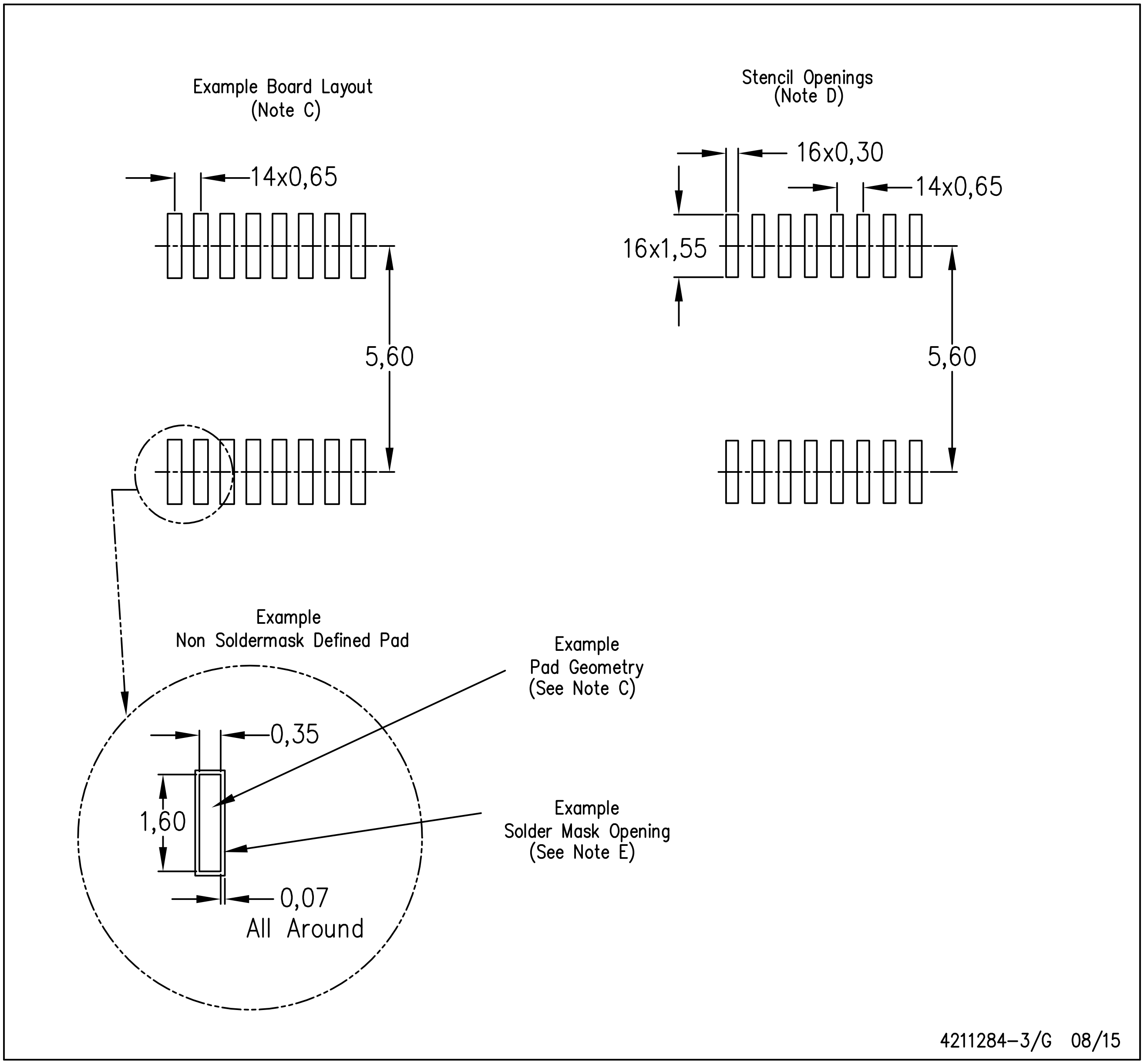
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

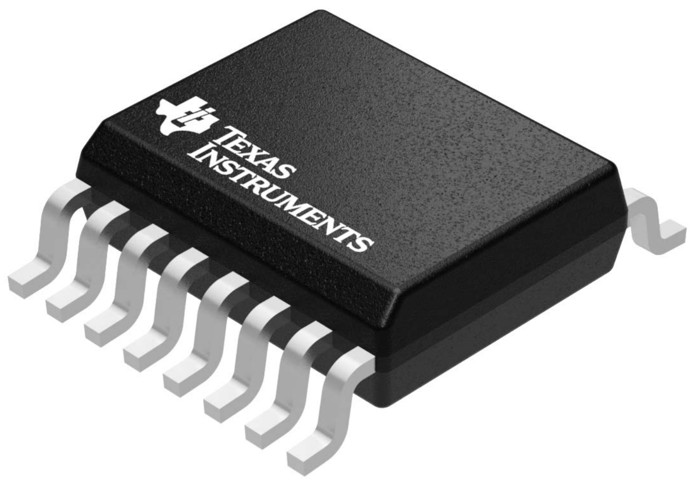
PW (R-PDSO-G16) PLASTIC SMALL OUTLINE



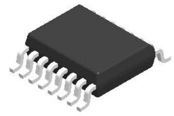
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

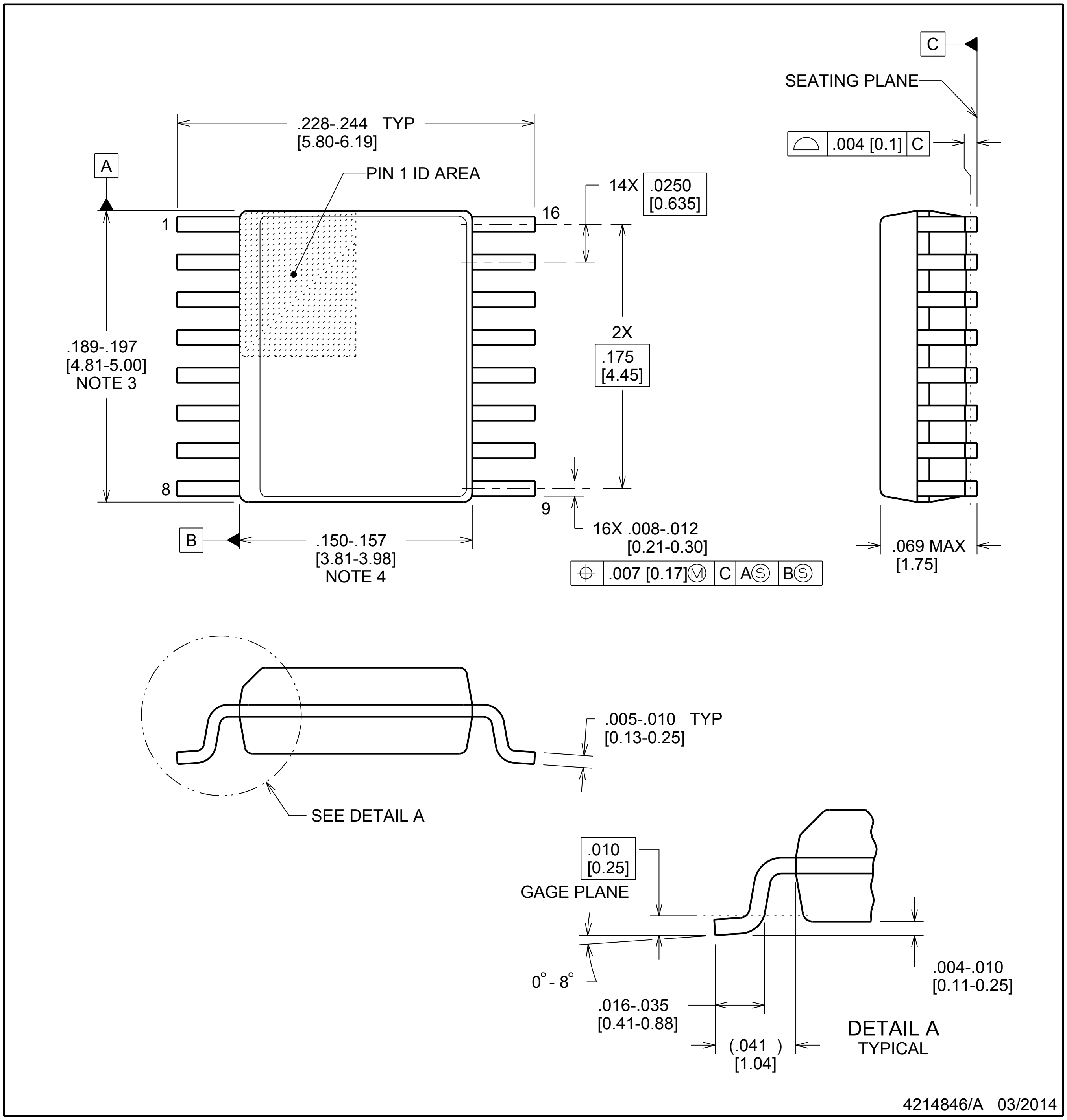
DBQ 16 — SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



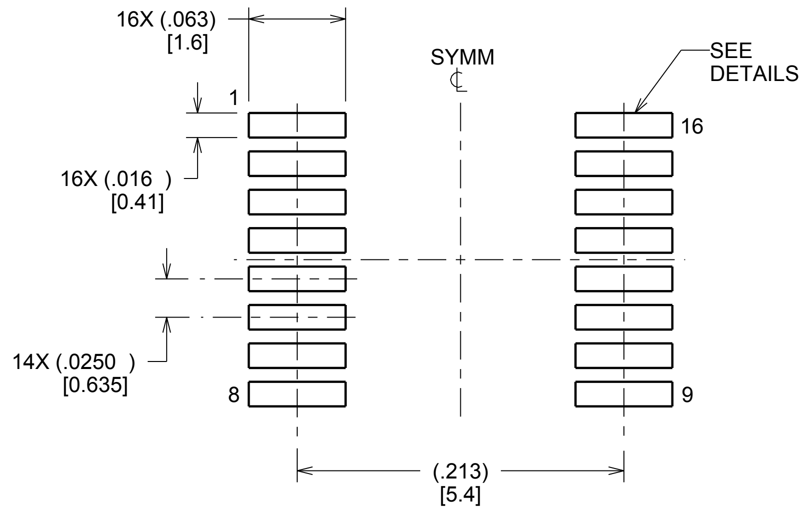
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



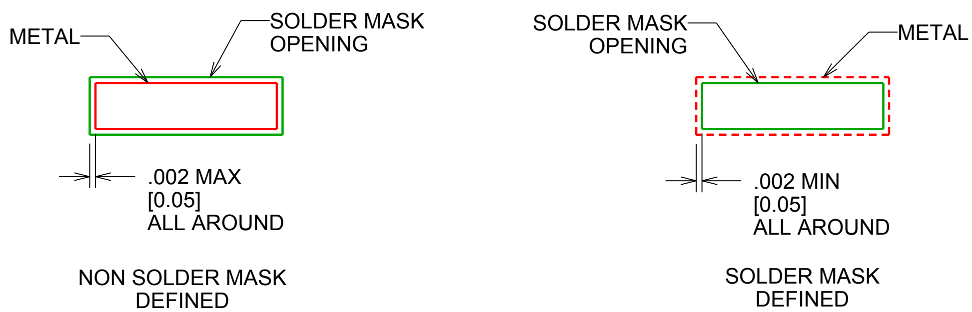


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

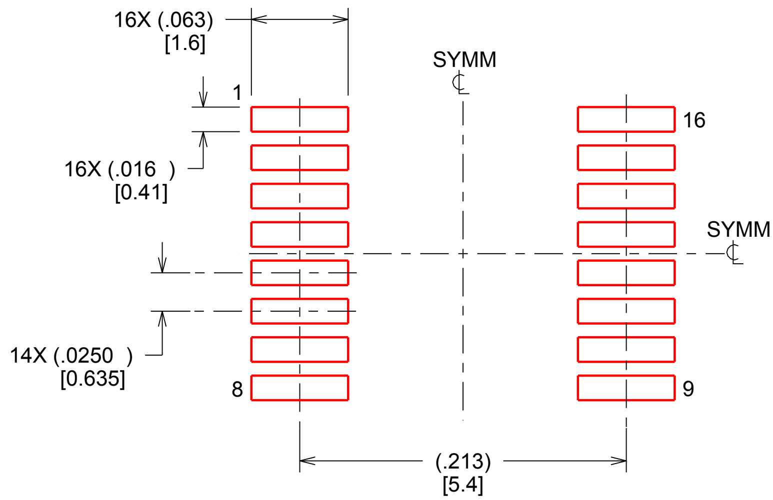


SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



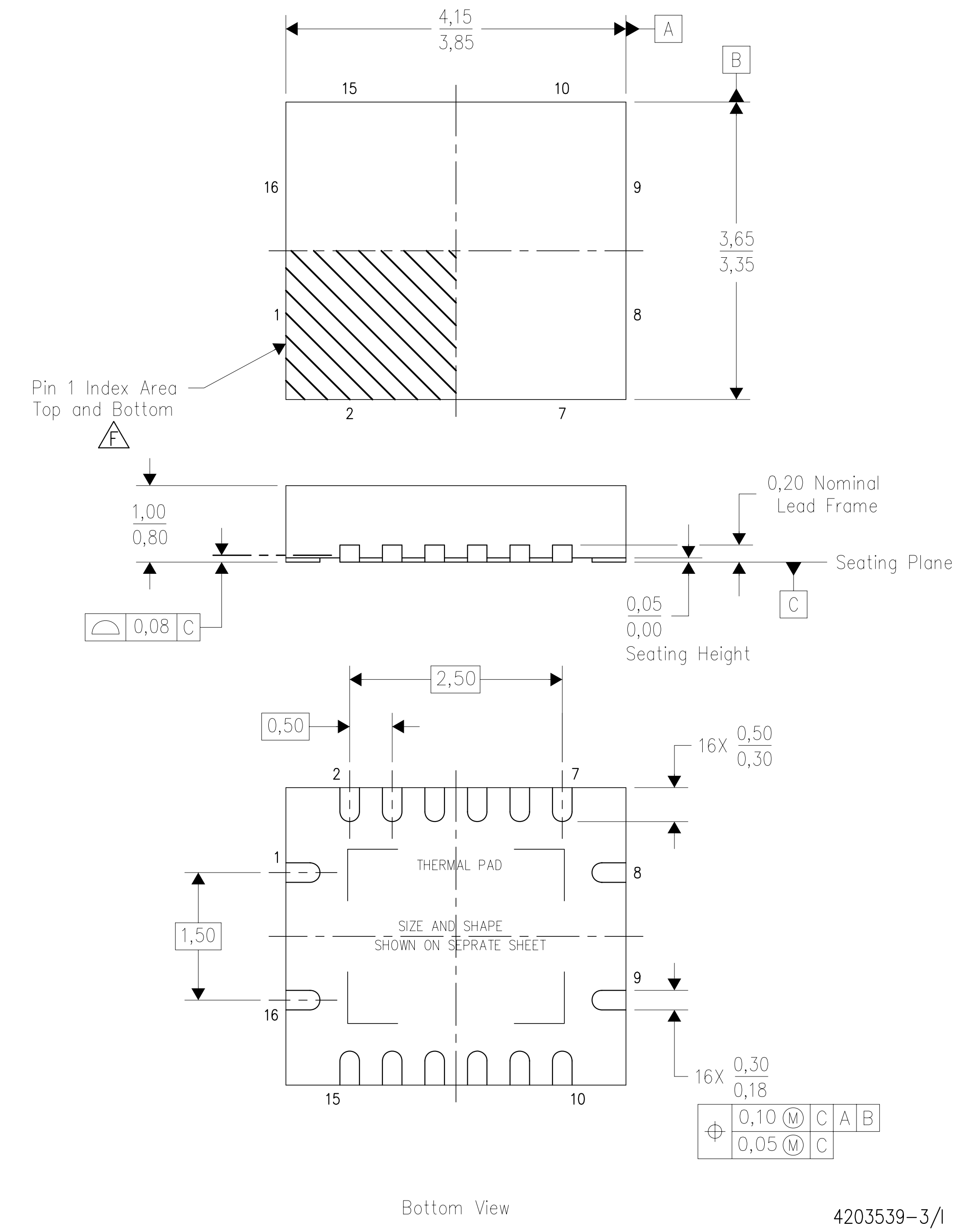
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



4203539-3/I 06/2011

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO–241 variation BA.

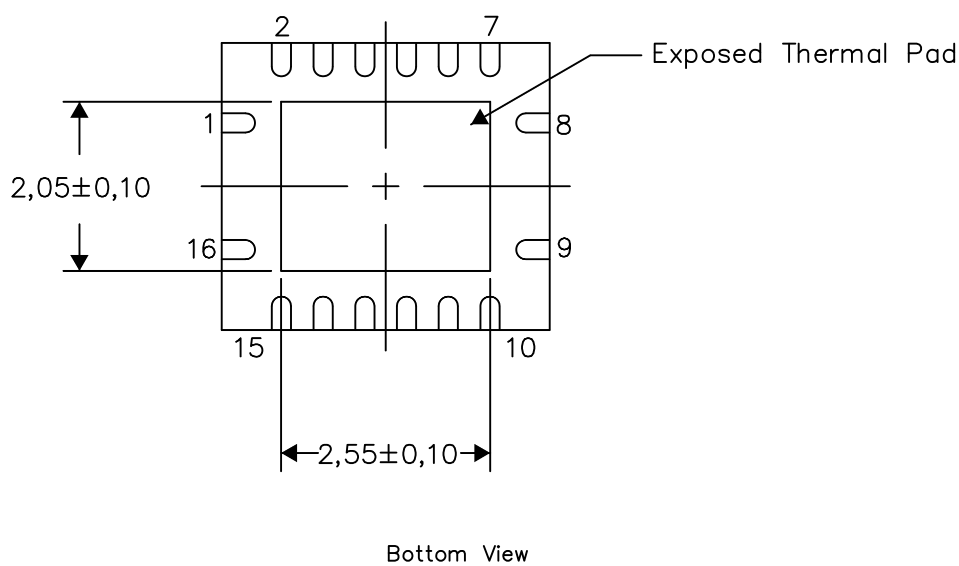
RGY (R-PVQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

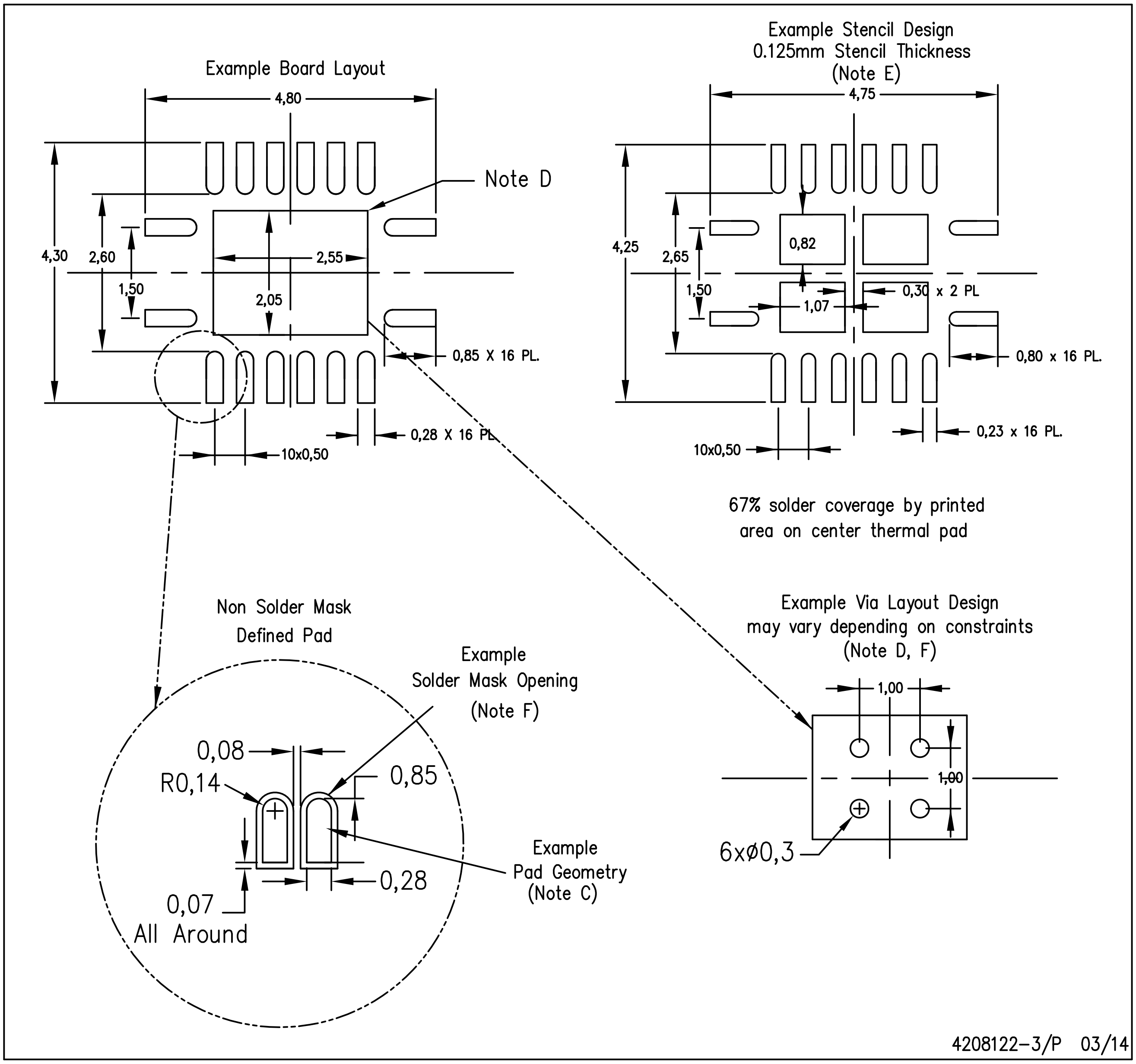


Exposed Thermal Pad Dimensions

4206353-3/P 03/14

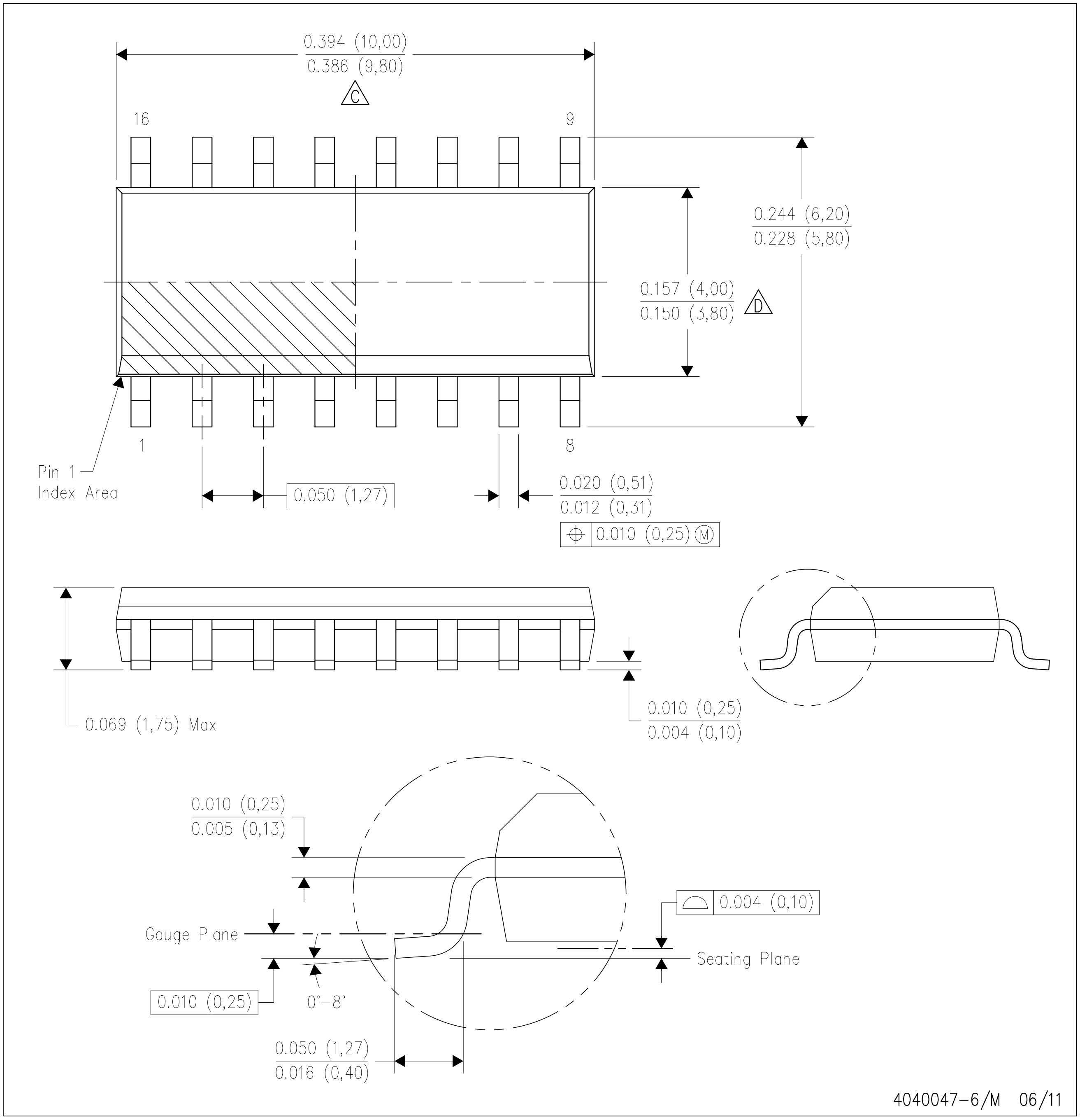
NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD



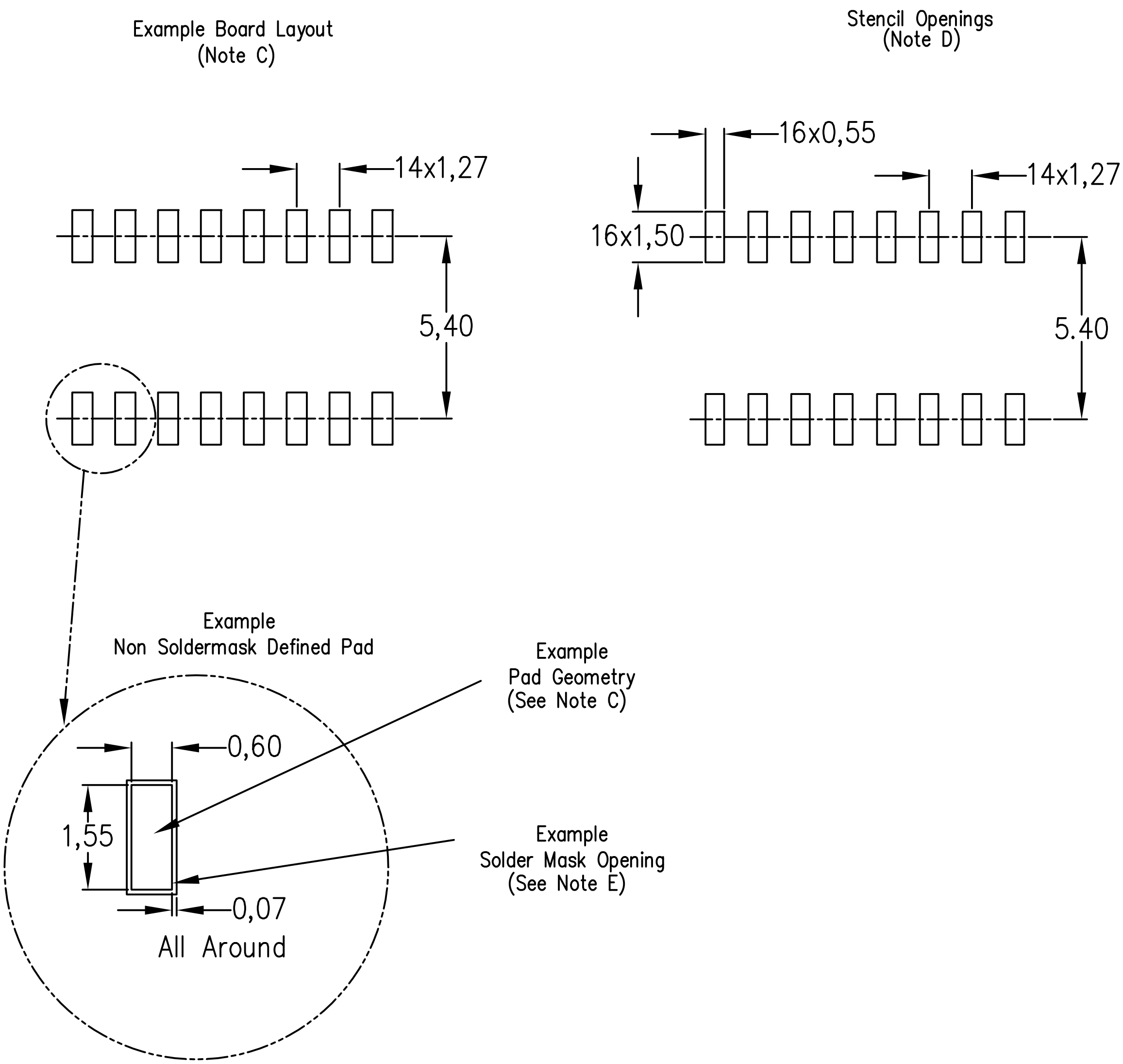
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AC.

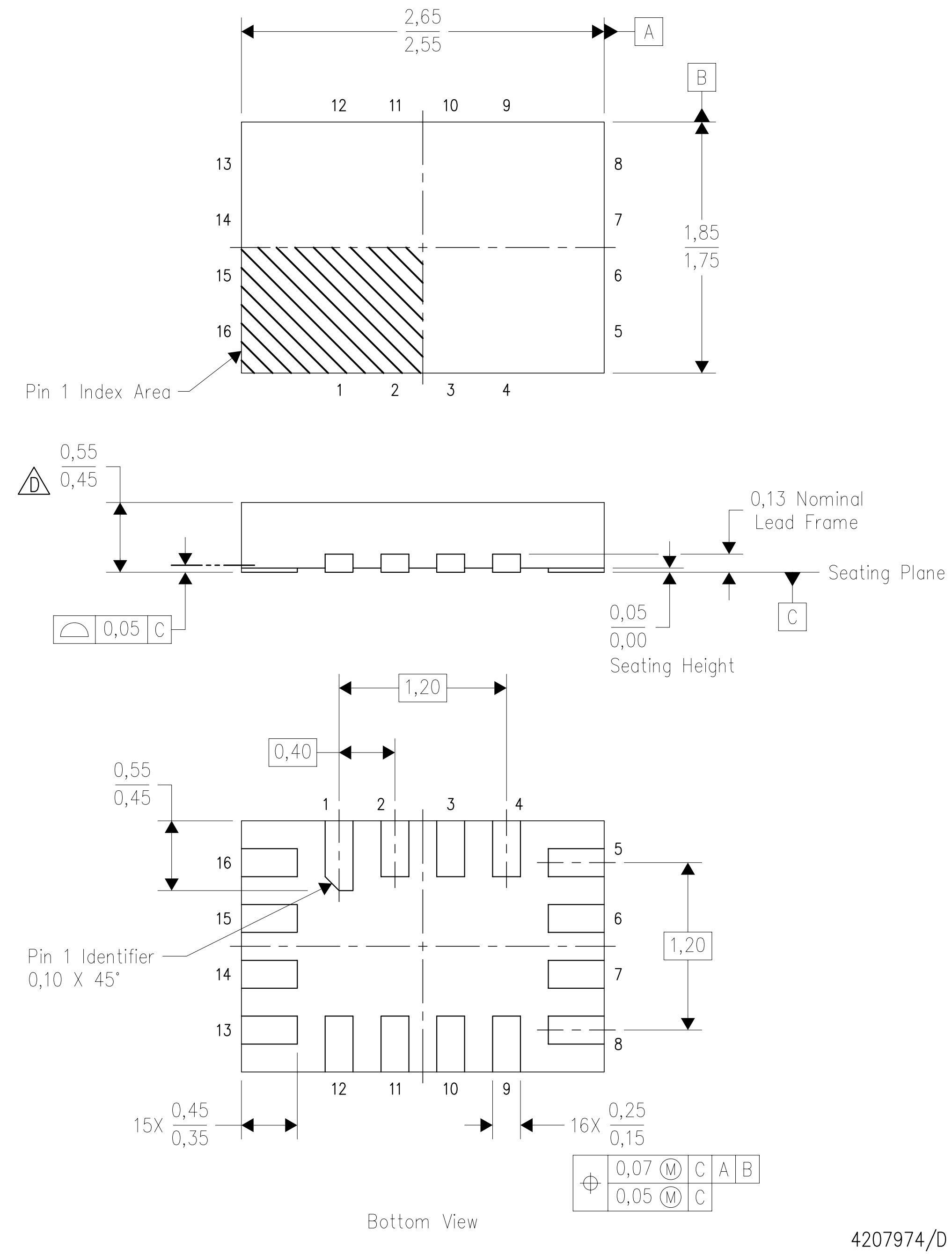
D (R–PDSO–G16) PLASTIC SMALL OUTLINE



4211283–4/E 08/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RSV (R–PUQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

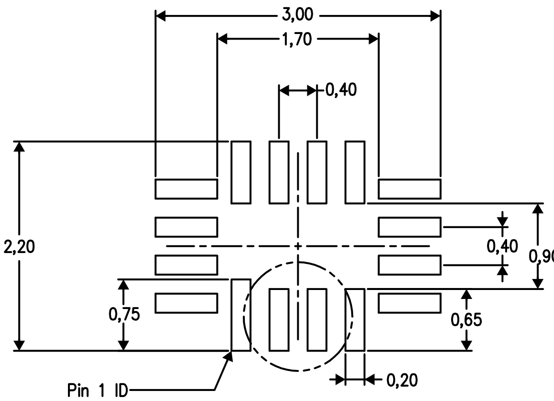


4207974/D 12/11

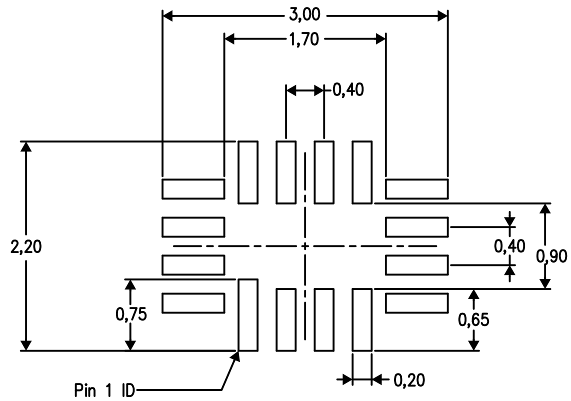
NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) package configuration.
- D. This package complies to JEDEC MO–288 variation UFHE, except minimum package thickness.

RSV (R–PUQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

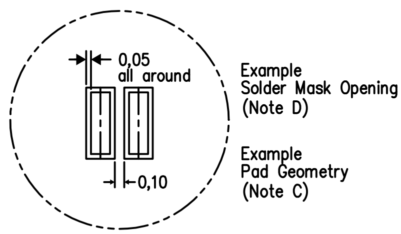
Example Board Layout



Example Stencil Design
0.125mm Stencil Thickness
(Note F&G)



Non Solder Mask Defined Pad

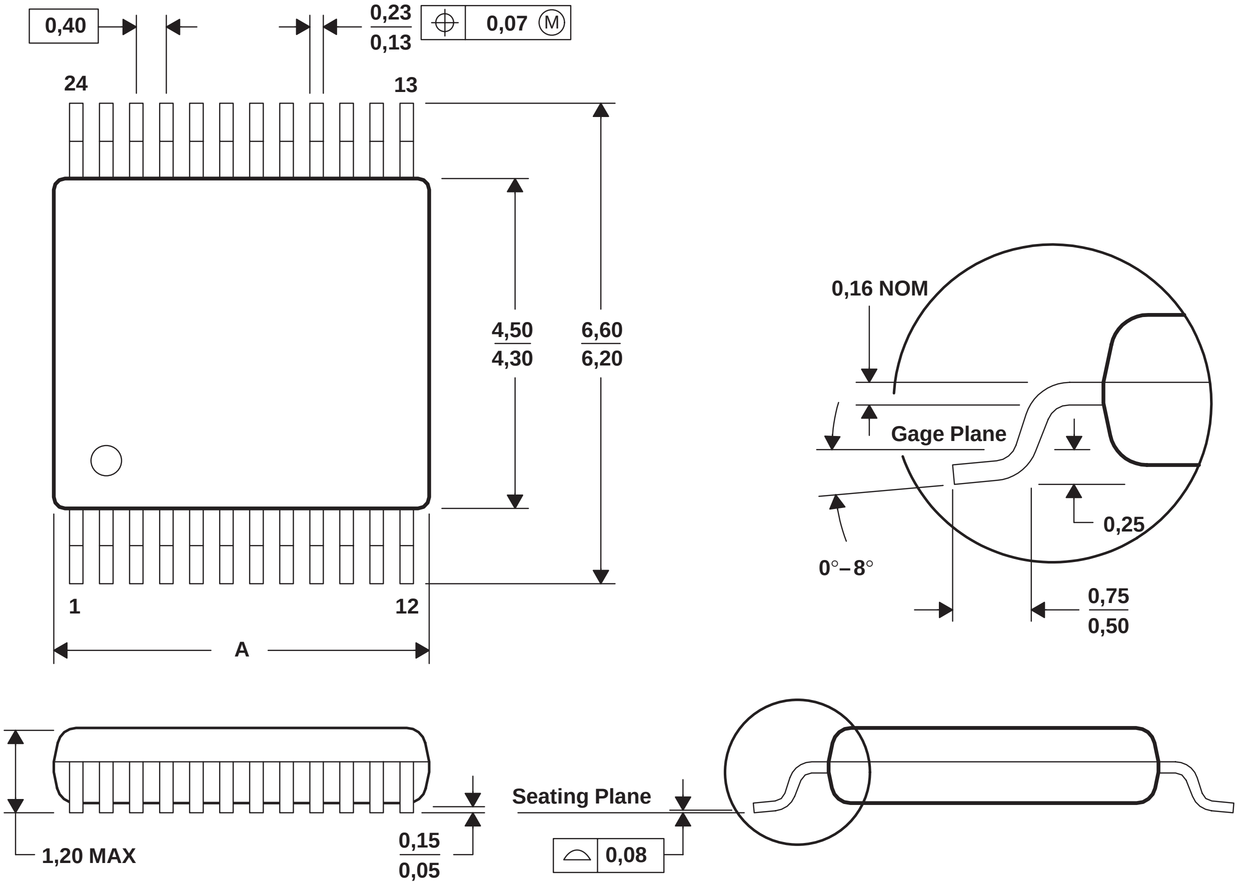


4208244/C 02/13

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



PINS ** / DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

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